REMARKS/ARGUMENTS

Reconsideration of the Application in view of the above amendments and the following remarks is respectfully requested.

The Examiner states that Figure 7-9 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. These Figures have been so amended. The Examiner's approval of the drawing changes is respectfully requested.

The Examiner rejects Claims 11-26 under U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The Examiner states that the added limitation to Claim 11 that "the wiring substrate having a single level of wiring and wherein the wiring on the wiring substrate is connected to the n-input terminals to couple data signals to the inputs of the switching circuits, the wires being parallel lines" was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art as the inventors at the time the application was filed had possession of the claimed invention. The Examiner states that they were not shown in the drawings.

This rejection is respectfully traversed. Page 9 of the specification at line 24 et seq recites impertinent part: "...the signal lines of data bus 200 wired on substrate 220 are wired...in which they are arranged parallel to each other without intersecting each other as shown in Figure 1, in substrate 220 data bus 200 can be formed by one-layer wiring.". See also Figures 1 and 5. Accordingly, there is clear support for this limitation in the claims, and applicants request that this rejection be withdrawn.

The Examiner states that newly added dependent claims 14, 17-18 and 25 were not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventors at the time of the application was filed had possession of the claimed invention.

Although the Examiner has not stated specifically what his rejection is based on, these claims all recite that the wiring for the first integrated circuit approaches the integrated circuit from a first direction and the wiring for a second integrated circuit approaches the integrated circuit from a second direction. Applicants believe that the problem results from the recitation of the term "perpendicular to" and this has been changed to --opposite-- in order to clarify these claims.

The Examiner states that newly added dependent claims 15, 19-21 and 26 wherein the wiring between the input terminals and the switching circuit comprises a continuous loop is not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventors at the time the application was filed had possession of the claimed invention.

Applicants have amended the claim in order to delete the term "loop" and substitute therefore --line--. This should overcome the Examiner's rejection.

The Examiner rejects Claims 11-12, 22-23 as best understood by the Examiner under 35 U.S.C. 103(a) as being unpatentable over Dingwall in view of Mical, et al. and further in view of Cha, et al. The Examiner rejects Claims 13, 16 and 24 as best understood by the Examiner under 35 U.S.C. 103(a) as being unpatentable over Dingwall , Cha, et al. and Mical, et al. as above and further in view of Viosin, et al.

We cannot agree. Dingwall shows, in the Figure 4 recited by the Examiner, the same technology shown in Figure 9 of the present application, which is acknowledged prior art. This only works where the inputs to the chip are on one of the long dimensions of the chip and the outputs are on the short dimensions of the chip (not shown in Figure 4 of Dingwall) which is not the case here. Because of the high switching frequency of the output lines, it is not practical to crowd them to have the inputs come along the short end of the chip and the outputs come along the long end of the chip in the present invention. These lines need greater spacing than this would provide. Furthermore, Mical is even further from the present invention. At top of col. 6 of Mical, is a description of a resolution-enhancing subsystem which includes a crossover unit 151 for selectively transposing part of the Px signals, first and second delay registers A and B couple to the crossover unit for generating previous column signals. Thus, although the reference mentions a cross-over unit, it is clear that this is for a completely different purpose and totally unrelated to the present invention. With respect to Cha, it is respectfully submitted that the wiring 30 and the wiring 20 are on different circuit boards which are attached to the integrated circuit chip 12 in Figure 1 and therefore comprise, in effect, a multilevel wiring, which is the problem sought to be overcome by the present invention. It should be noted that Claim 11 recites a wiring substrate having a single level of wiring thereon.

Claim 11 has been amended in several respects. First of all, the outputs have been changed so that instead of reciting "n" output terminals, we now recite "m" output terminals. This is to avoid the suggestion that the number of input terminals and output terminals must be the same, which is clearly not necessary in the present invention. In addition, Claim 11 has been amended to recite that each of the integrated circuits have the inputs arranged linearly in a row along a first side and the outputs arranged on a second side parallel to the first side where the second side faces the display device and

the first side faces away from the display device, which clearly distinguishes over the references cited by the Examiner. This renders Claims 12 and 23 superfluous and they have been canceled without prejudice.

Accordingly, Applicants believe that the Application, as amended, is in condition for allowance, and such action is respectfully requested.

Respectfully submitted,

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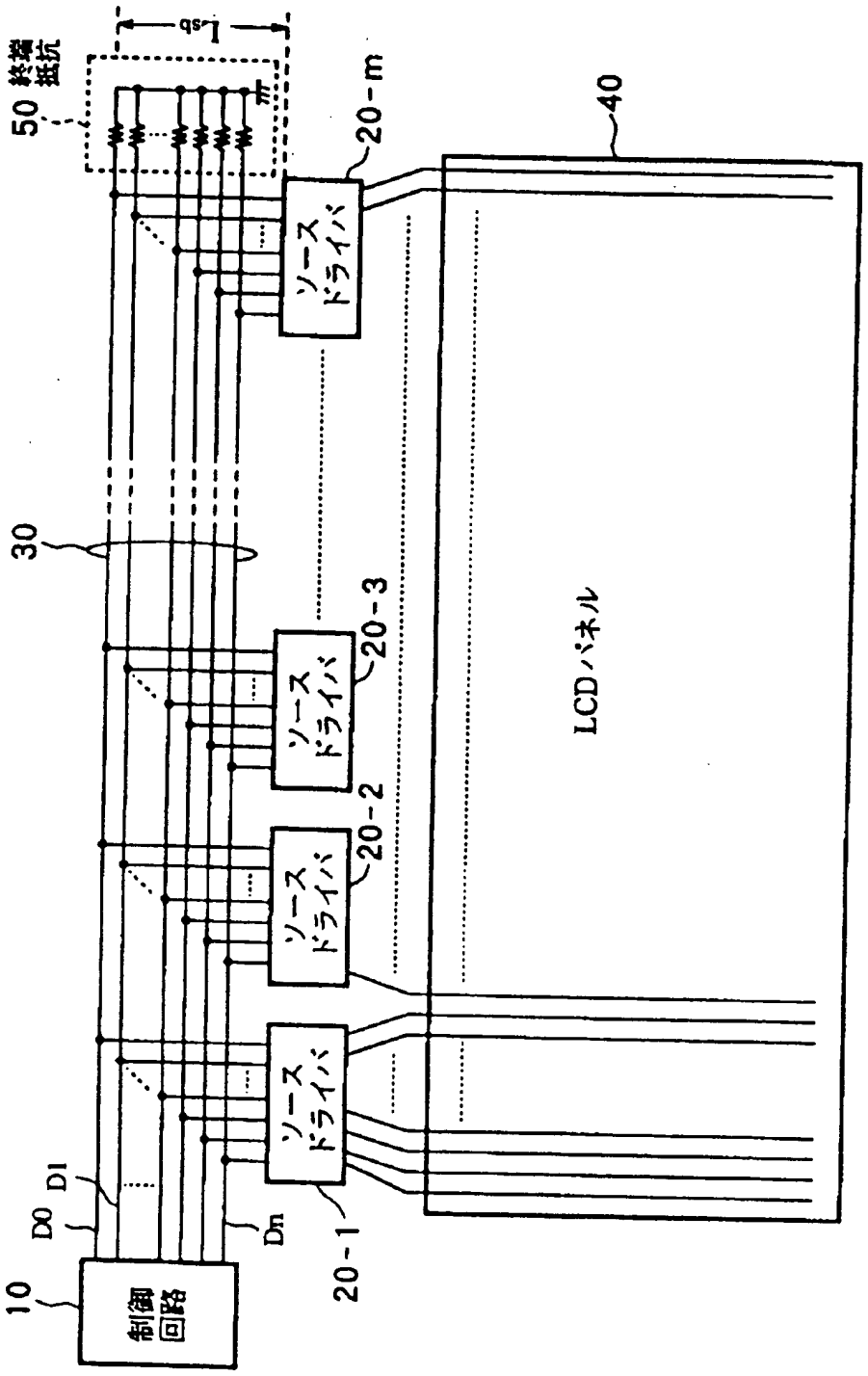
【図7】

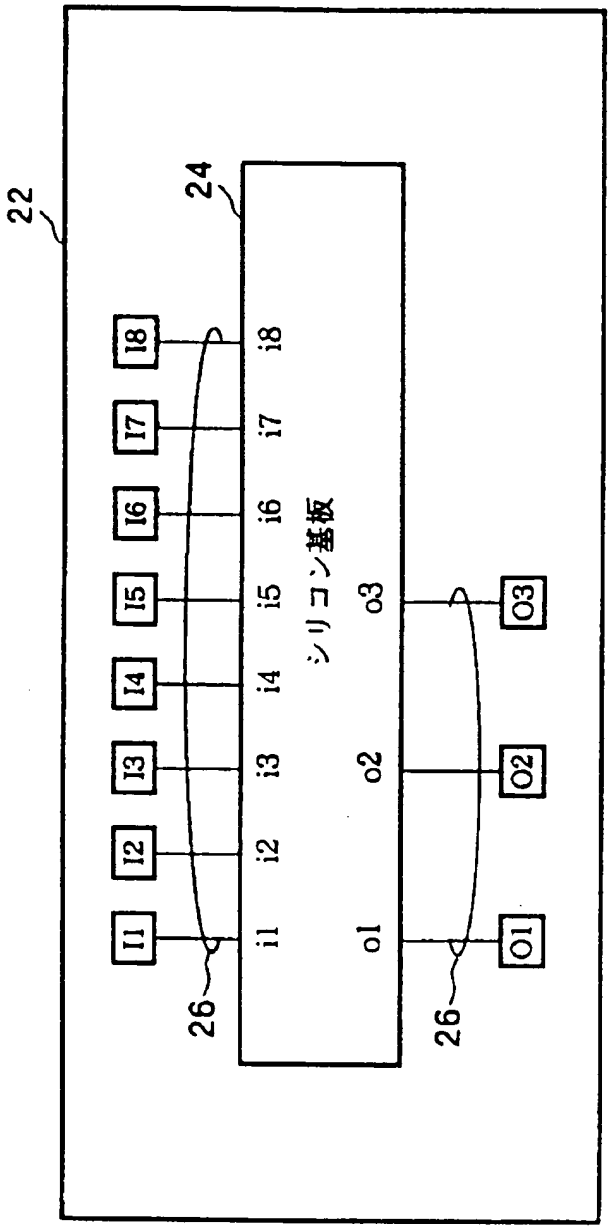


PRIOR ART

Approved by examiner L.S. 12.08.03

【図８】

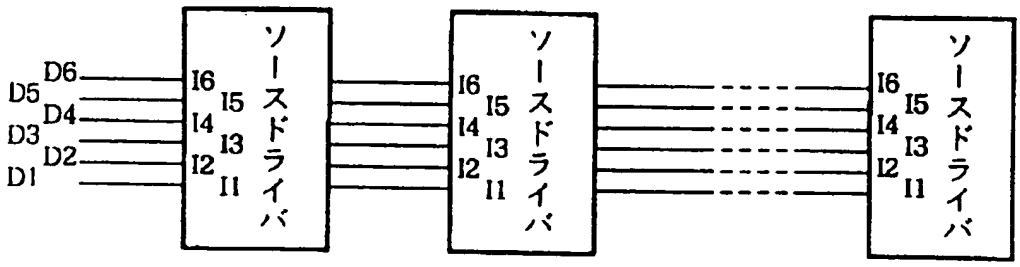
Appl. No. 09/742,036
Amdt. dated 08/21/2003
Reply to Office action of 07/02/2003



PRIOR ART

【図9】

Appl. No. 09/742,036
Amdt. dated 08/21/2003
Reply to Office action of 07/02/2003



PRIOR ART